WHAT IS CLAIMED IS:

1. An off-chip driver circuit having first to N^{th} off-chip drivers for using a data signal and first to N^{th} control signals respectively to determine whether to produce output signals according to corresponding control signals, being characterized in that:

at least one of the first to N^{th} off-chip drivers comprises a delay circuit(s) for outputting a signal having a given delay time compared with other signals of the remaining off-chip drivers.

2. The off-chip driver circuit as claimed in claim 1, wherein the delay circuit is added to an input terminal of the off-chip driver to delay the data signal.

3. The off-chip driver circuit as claimed in claim 1, wherein the delay circuit is added to an output terminal of the off-chip driver to delay the output signals.

4. The off-chip driver circuit as claimed in claim 1, wherein each of the off-chip drivers performs an NAND operation for a corresponding control signal and the data signal when a logical status of the inputted data signal is High, and an NOR operation for an inverse signal of a corresponding control signal and the data signal when a logical status of the inputted data signal is Low.

control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver is driven.

6. A data output circuit, comprising:

first to N^{th} off-chip drivers for outputting a data signal, respectively, in response to corresponding first to N^{th} control signals;

a pre-driver circuit for using the data signal to drive an output driver circuit; and

the output driver circuit connected to the outputs of the off-chip driver circuit and the pre-driver circuit,

wherein at least one of the first to N^{th} off-chip drivers comprises a delay circuit for delaying the data signal.

7. The data output circuit as claimed in claim 6, wherein the pre-driver circuit receives the data signal and pulls up or pulls down according to a logical status of the data signal.

8. The data output circuit as claimed in claim 6, wherein each of the off-chip drivers performs an NAND operation for a corresponding control signal and the data signal when a logical status of the inputted data signal is High, and an NOR operation for an inverse signal of a corresponding control signal and the data signal when a logical status of the inputted data signal is Low.

9. The data output circuit as claimed in claim 8, wherein the output driver circuit comprises each of the output drivers and off-chip drivers corresponding to the pre-driver circuit, wherein if a control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver is driven.